In this sketch we propose a scalable tightly coupled cluster of hardware for parallel rendering. Most importantly the interconnect implements a Distributed Shared Memory (DSM) architecture in hardware. Figure 2 shows how local memories on the custom-built boards and the PCs become part of the system wide DSM through the SCI interconnect. Figure 2 also depicts Field Programmable Gate Arrays (FPGAs) on the custom-built boards. These reconfigurable components assist the SCI implementation and provide substantial additional computational resources that may be used to control the commodity graphics accelerators and to perform operations associated with a parallel rendering infrastructure. Beyond the previously mentioned application of the FPGAs we envision other graphics application related computation e.g., ray tracing. These reconfigurable components are an integral part of the scalable shared-memory graphics cluster and consequently increase the programmability of the parallel rendering system, just like vertex and pixel shaders increased the programmability of graphics pipelines.

Figure 2: Shared memory system.

In this sketch we describe the design of a tightly coupled scalable Non-Uniform Memory Access (NUMA) architecture of distributed FPGAs, GPUs and memory that may be constructed with a limited amount of custom-built hardware. A first prototype of the custom-built boards, seen in Figure 1, was manufactured and is currently debugged. A second revision will resolve outstanding problems. We expect that this hardware DSM cluster communicates data at 500Mbytes/s with low latencies (< 1.5 μs). This hard real-time capable parallel rendering cluster will be connected with the same high speed interconnect to a commodity PC cluster that will execute the graphics application. We have introduced this novel architecture and estimate, based on the arguments presented, that this solution could out-perform pure commodity implementations without increased hardware cost and yet maintain its adaptability to the most recent generation of commodity graphics accelerators and target applications. Later prototypes will incorporate PCI Express to be compatible with the latest commodity graphics accelerators. 

References